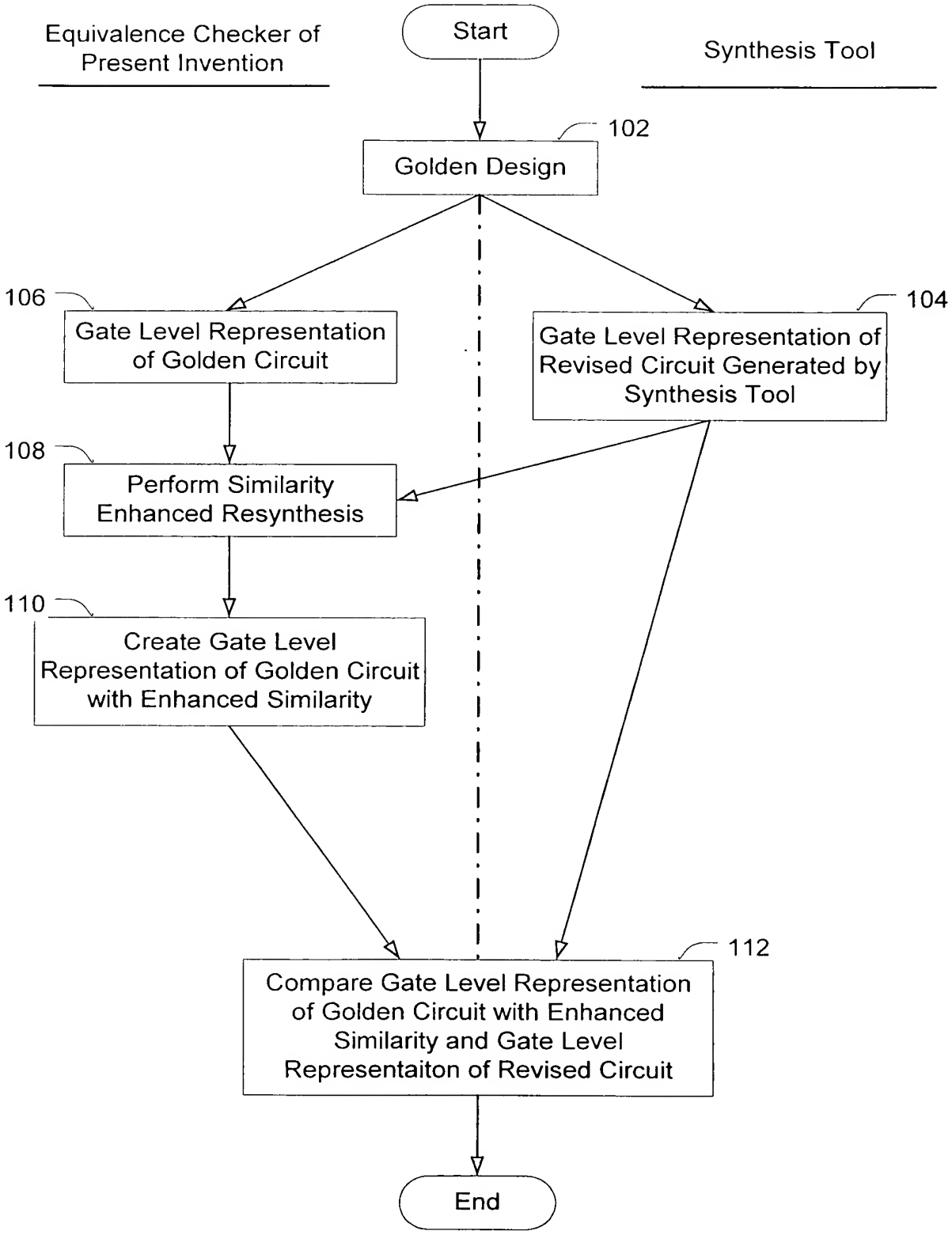
Equivalence Checker of Present Invention
Start
Synthesis Tool
102
Golden Design
106
Gate Level Representation of Golden Circuit
104
Gate Level Representation of Revised Circuit Generated by Synthesis Tool
108
Perform Similarity Enhanced Resynthesis
110
Create Gate Level Representation of Golden Circuit with Enhanced Similarity
112
Compare Gate Level Representation of Golden Circuit with Enhanced Similarity and Gate Level Representaiton of Revised Circuit
End

Fig. 1

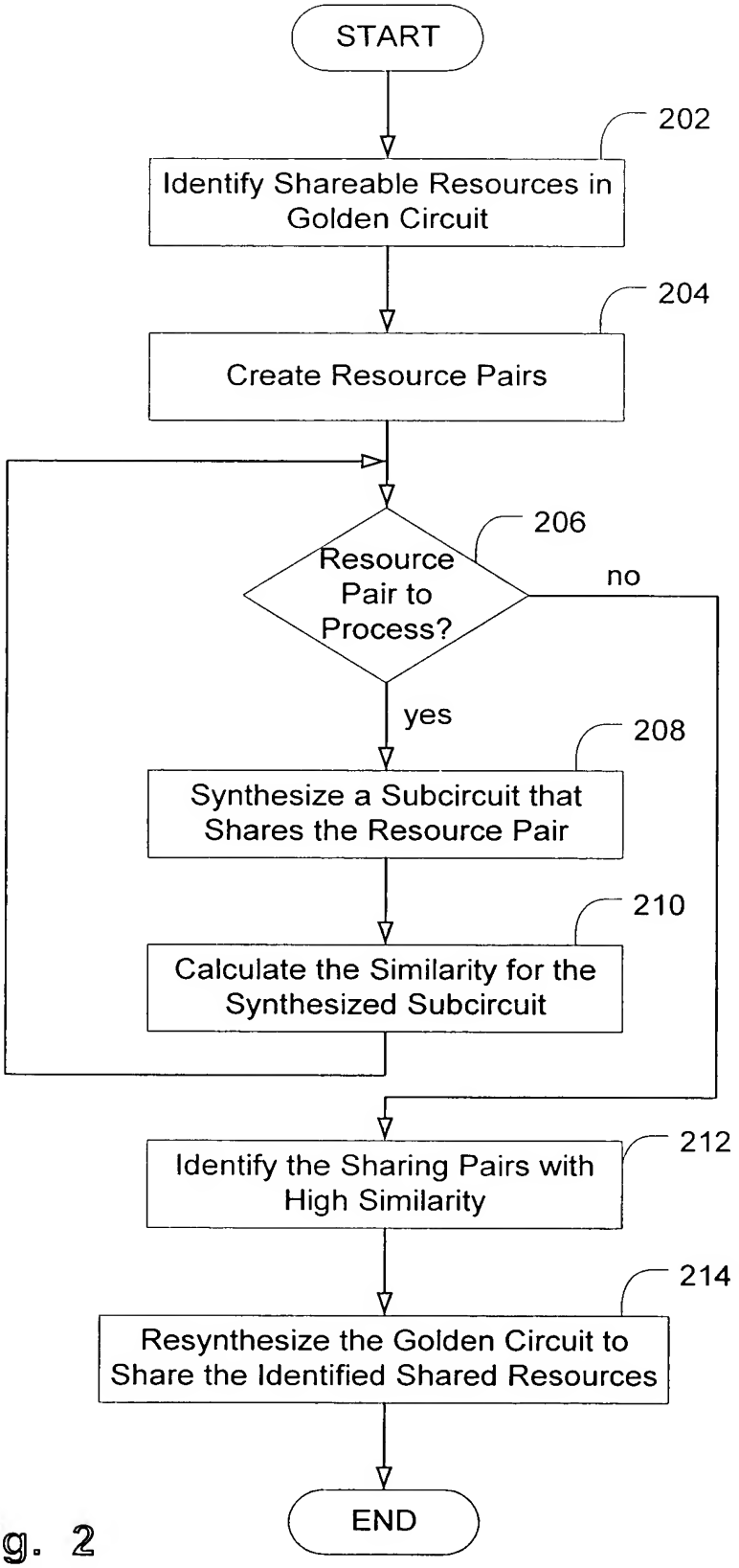
START
202
Identify Shareable Resources in Golden Circuit
204
Create Resource Pairs
206
Resource Pair to Process?
no
yes
208
Synthesize a Subcircuit that Shares the Resource Pair
210
Calculate the Similarity for the Synthesized Subcircuit
212
Identify the Sharing Pairs with High Similarity
214
Resynthesize the Golden Circuit to Share the Identified Shared Resources
END

Fig. 2

Verilog Example For Resource Sharing Learning

```
module example(in1,in2,in3,in4,in5,in6,in7,in8,sel,y);
input [3:0] in1,in2,in3,in4,in5,in6,in7,in8;
input [2:0] sel;
output [7:0] y;
reg [7:0] y;

always @(in1 or in2 or in3 or in4 or in5 or in6 or in7 or in8 or sel) begin
   case(sel)
      1:
         y = in1 * in2;      // multiplier m1
      2:
         y = in3 * in4;      // multiplier m2
      3:
         y = in5 * in6;      // multiplier m3
      default:
         y = in7 * in8;      // multiplier m4
   endcase
end

endmodule
```

Fig. 3

(a) Sharing Pair Examples

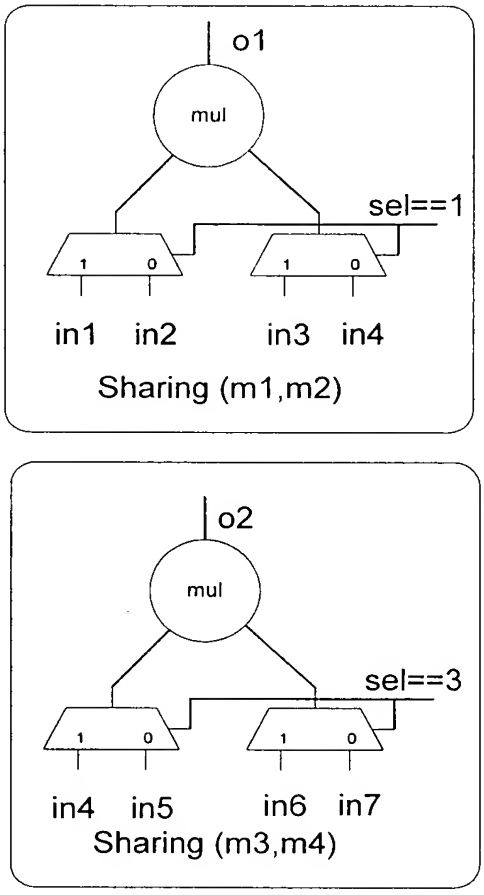

Fig. 4A

(b) Golden Circuit

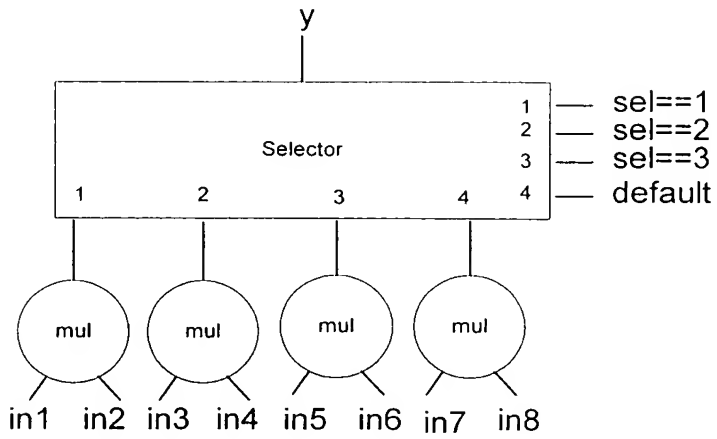

Fig. 4B

(c) Revised Circuit

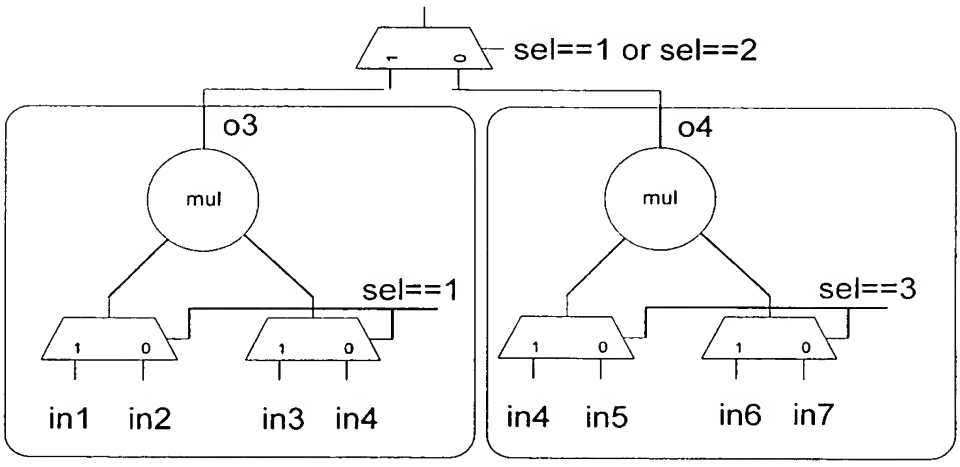

Fig. 4C

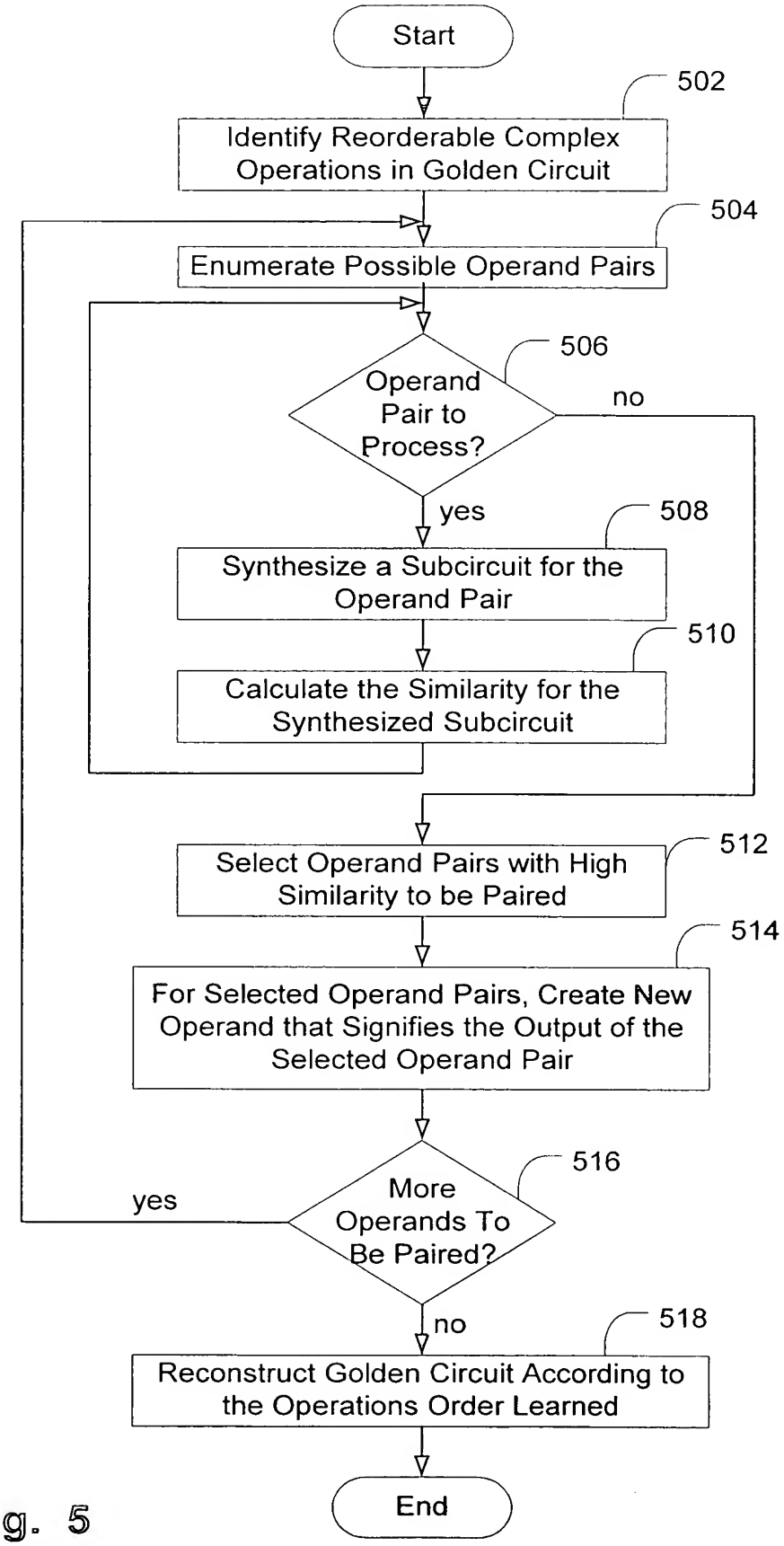
Start
502
Identify Reorderable Complex Operations in Golden Circuit
504
Enumerate Possible Operand Pairs
506
Operand Pair to Process?
no
yes
508
Synthesize a Subcircuit for the Operand Pair
510
Calculate the Similarity for the Synthesized Subcircuit
512
Select Operand Pairs with High Similarity to be Paired
514
For Selected Operand Pairs, Create New Operand that Signifies the Output of the Selected Operand Pair
516
More Operands To Be Paired?
yes
no
518
Reconstruct Golden Circuit According to the Operations Order Learned
End

Fig. 5

(a) Golden Netlist

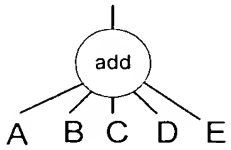

Fig. 6A

(b) Revised Netlist

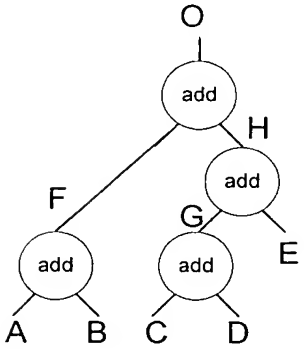

Fig. 6B

(c) Learning Steps

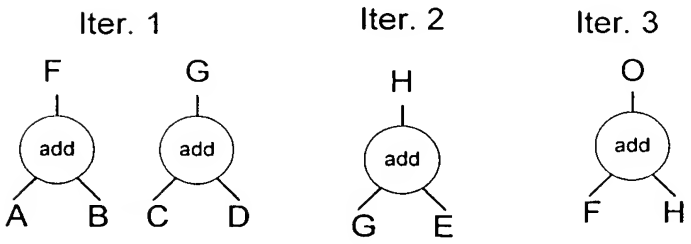

Fig. 6C

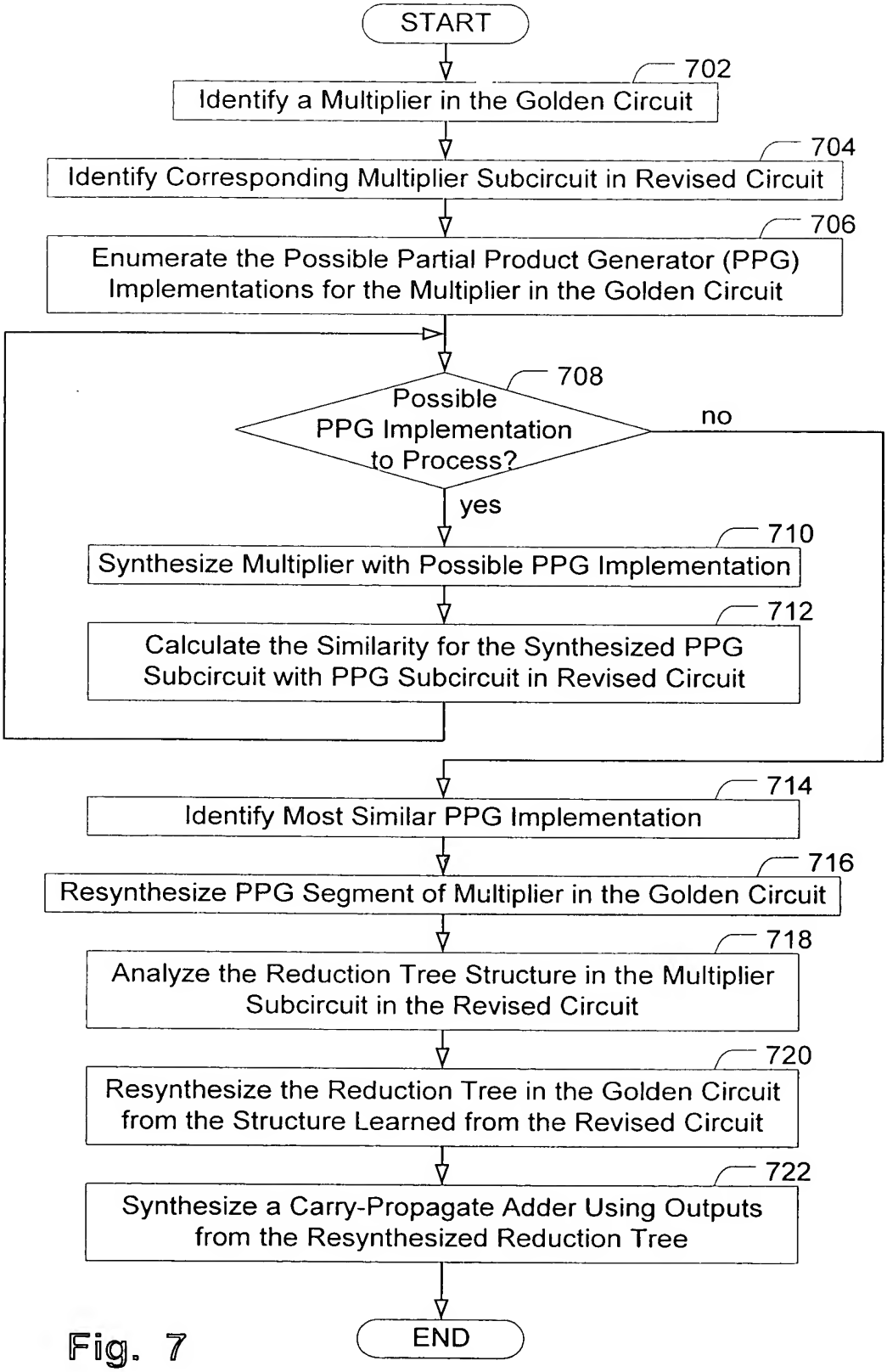
START
702
Identify a Multiplier in the Golden Circuit
704
Identify Corresponding Multiplier Subcircuit in Revised Circuit
706
Enumerate the Possible Partial Product Generator (PPG) Implementations for the Multiplier in the Golden Circuit
708
Possible PPG Implementation to Process?
no
yes
710
Synthesize Multiplier with Possible PPG Implementation
712
Calculate the Similarity for the Synthesized PPG Subcircuit with PPG Subcircuit in Revised Circuit
714
Identify Most Similar PPG Implementation
716
Resynthesize PPG Segment of Multiplier in the Golden Circuit
718
Analyze the Reduction Tree Structure in the Multiplier Subcircuit in the Revised Circuit
720
Resynthesize the Reduction Tree in the Golden Circuit from the Structure Learned from the Revised Circuit
722
Synthesize a Carry-Propagate Adder Using Outputs from the Resynthesized Reduction Tree
END

Fig. 7

Multiplier Example P[6:0] = A[3:0] * B[2:0]

Column	6	5	4	3	2	1	0
Weight	2^6	2^5	2^4	2^3	2^2	2^1	2^0

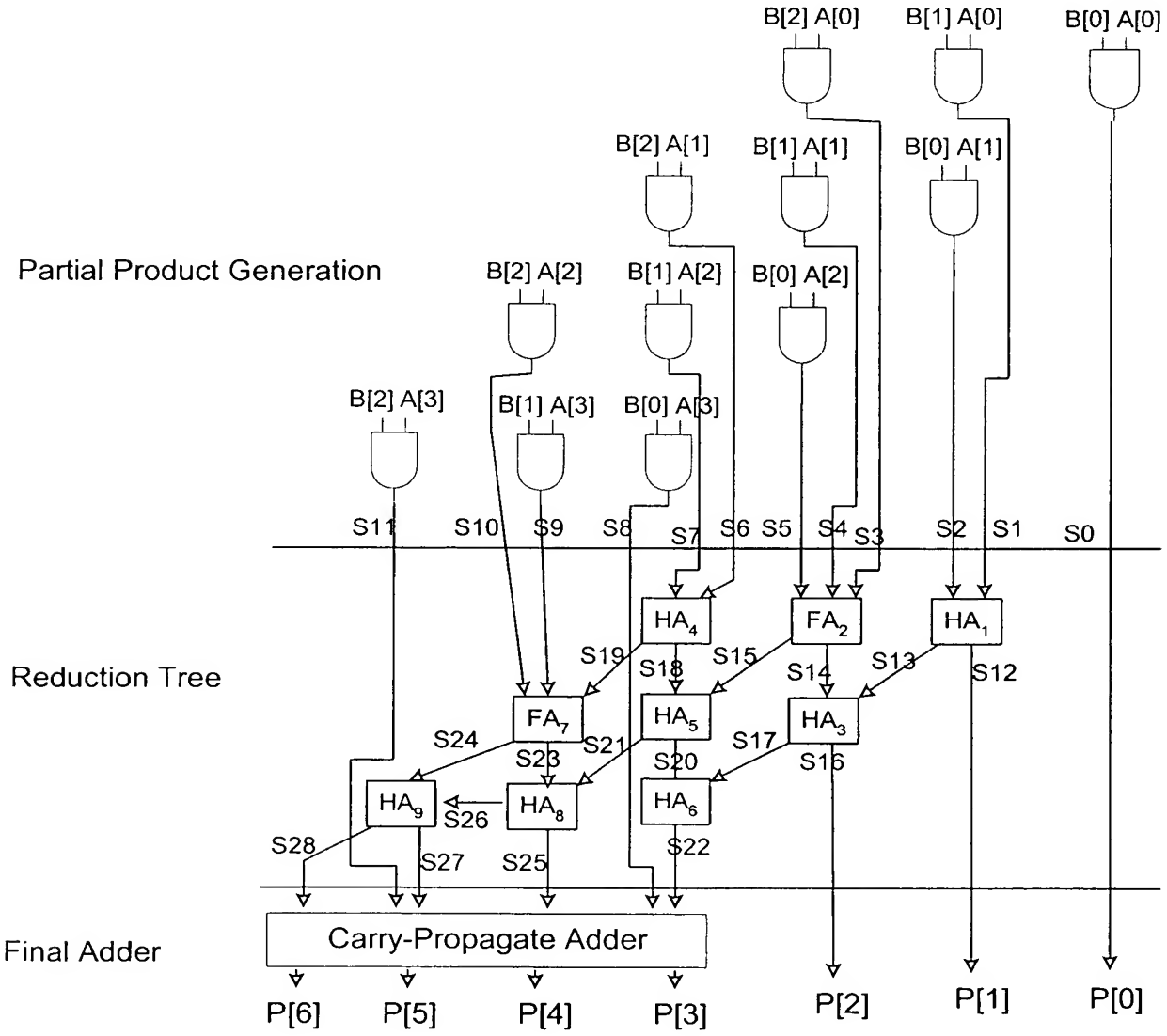

Fig. 8